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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/761,782

01/20/2004

Duc Ho

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7590

06/17/2004

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EXAMINER

NGUYEN, TAN

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

8

Office Action Summary

Application No.

10/761,782

Applicant(s)

HO ET AL.

Examiner

Tan T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 39-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 45-55 is/are allowed.
- 6) ☒ Claim(s) 39-44, 56, 59 and 60 is/are rejected.
- 7) ☒ Claim(s) 57, 58 and 61-64 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>01/20/04</u> . | 6) <input type="checkbox"/> Other: _____ |

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1. The Preliminary amendment filed by Applicants on January 20, 2004 has been received and entered.

2. The Information Disclosure Statement submitted by Applicants on January 20, 2004 has been received and fully considered.

3. Claims 1-38 have been canceled.

New claims 39-64 have been added.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 39-44, 56, 59-60 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 18-22 of U.S. Patent No. 6,707,722. Although the conflicting claims are not identical, they are not patentably distinct from each other because regarding claims 39 and 56 of the present application, claim 18 of U.S. Patent No. 6,707,722 recited a method for controlling (regulating) a maximum gate voltage of an output element in an output buffer comprising the steps of receiving a control signal at a control terminal of a predriver pull-up device of a predriver circuit, providing the maximum gate voltage from the predriver

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pull-up device to a limiter circuit, the limiter circuit configured between the predriver pull-up device and the output element, limiting the maximum gate voltage provided through the limiter circuit to the output element. The maximum gate voltage input to and output from the limiter circuit would be understood as the claimed output voltage from the predriver to the limiter circuit and the claimed control voltage provided to the output element in an output buffer in claim 39. Although claim 18 of U.S. Patent No. 6,707,722 does not include the step of driving the output element with the control voltage but it is inherent that the maximum gate voltage provided through the limiter circuit is used to drive the output element in the output buffer. Furthermore, claim 18 of U.S. Patent No. 6,707,722 does not recite in detail the limiter circuit limit the maximum gate voltage to no greater than a maximum voltage level, but the limiter circuit inherently sets a maximum voltage level to which the maximum gate voltage is limited under.

Regarding claims 40 and 59 of the present application, claim 19 of U.S. Patent No. 6,707,722 recited the step of limiting the maximum gate voltage comprises limiting the maximum gate voltage to an amount not greater than an internally regulated voltage less a threshold voltage of the limiter circuit.

Regarding claim 41 of the present application, claim 20 of U.S. Patent No. 6,707,722 recited the method further comprises the step of reducing a maximum current in an I-V characteristic of the output element.

Regarding claims 42-44 and 60 of the present Application, claims 21-22 of U.S. Patent No. 6,707,722 recited the step of limiting the maximum gate voltage comprises limiting the maximum gate voltage through clamping of the maximum gate voltage

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based on a diode configuration of the limiter circuit, or of a plurality of diode-connected p-channel transistors and a plurality of diode-connected n-channel transistors.

6. Claims 57-58, 61-64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 45-55 are allowed.

8. The following is an examiner's statement of reasons for allowance:

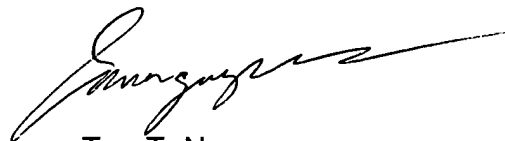
The prior art failed to show or suggest the limitation of an output pull-down element of the output buffer as claimed in claims 45 and 52. The prior art also failed to show or suggest the limitation of providing the output voltage from a drain terminal of the predriver transistor device as claimed in claims 57-58, or clamping the output voltage from the drain terminals of a p-channel predriver device as claimed in claims 61-64.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached at (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2818
June 15, 2004